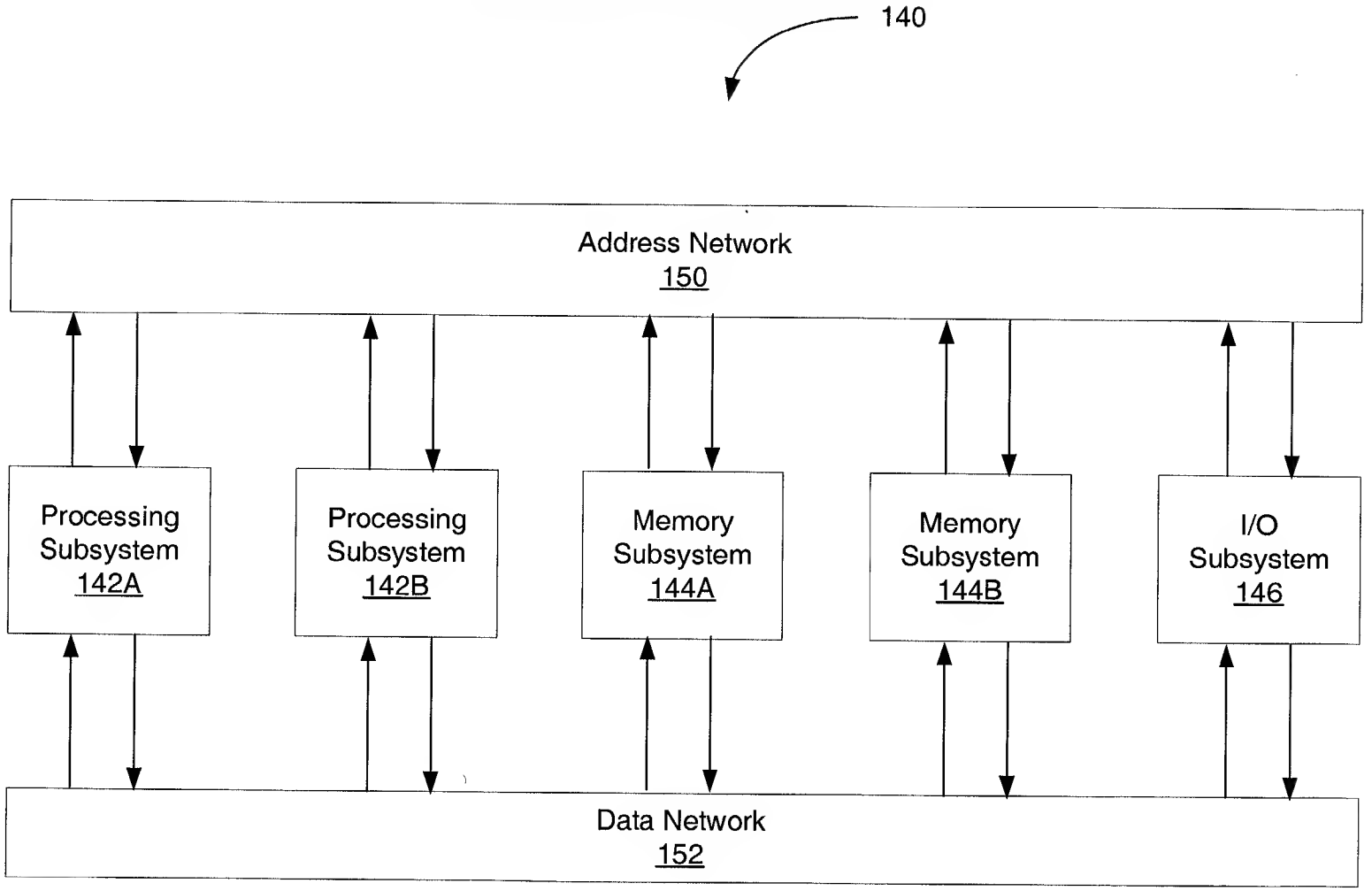


Fig. 1

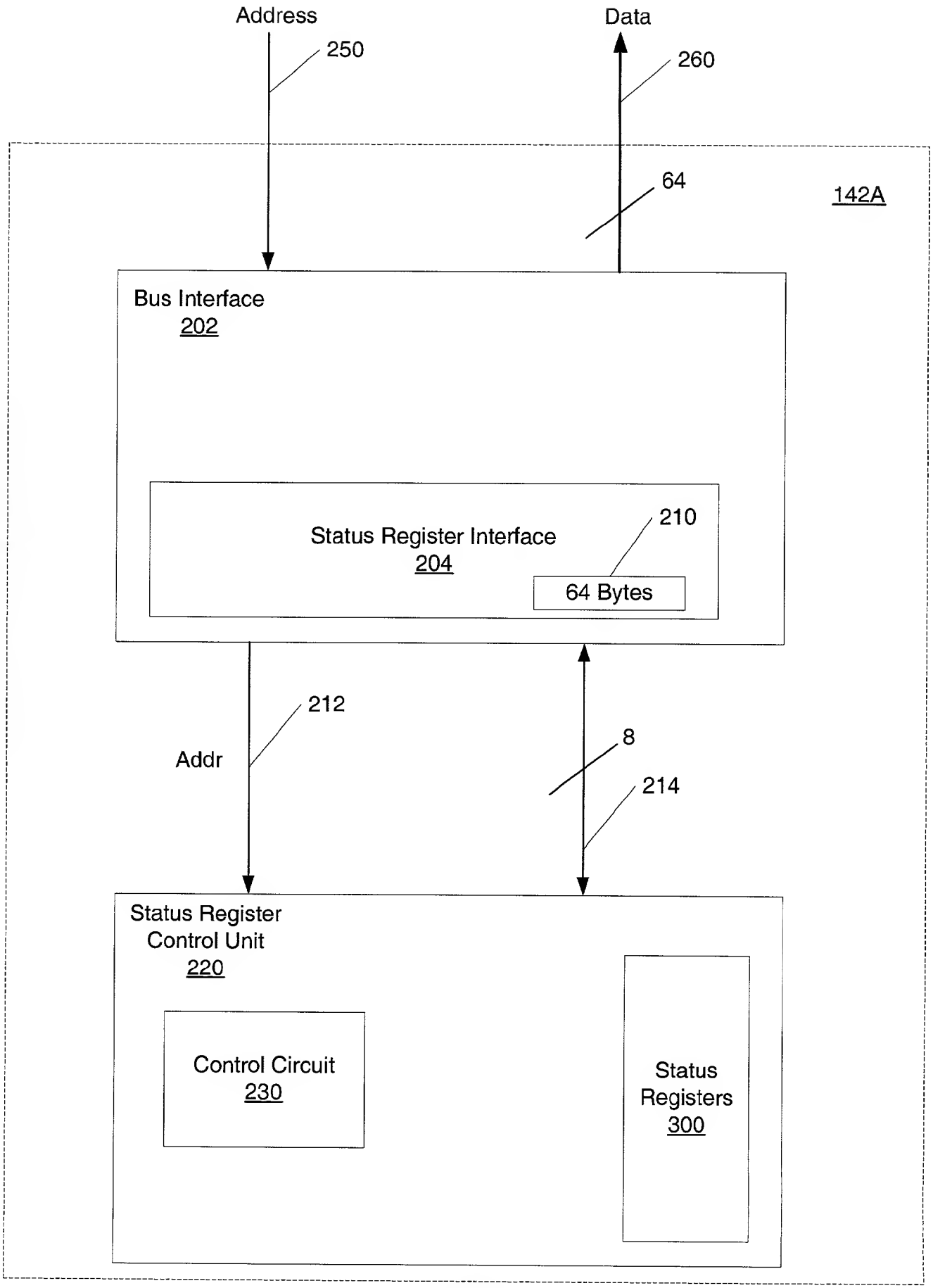

Address
250
Data
260
64
142A
Bus Interface
202
Status Register Interface
204
210
64 Bytes
212
Addr
8
214
Status Register
Control Unit
220
Control Circuit
230
Status
Registers
300

Fig. 2

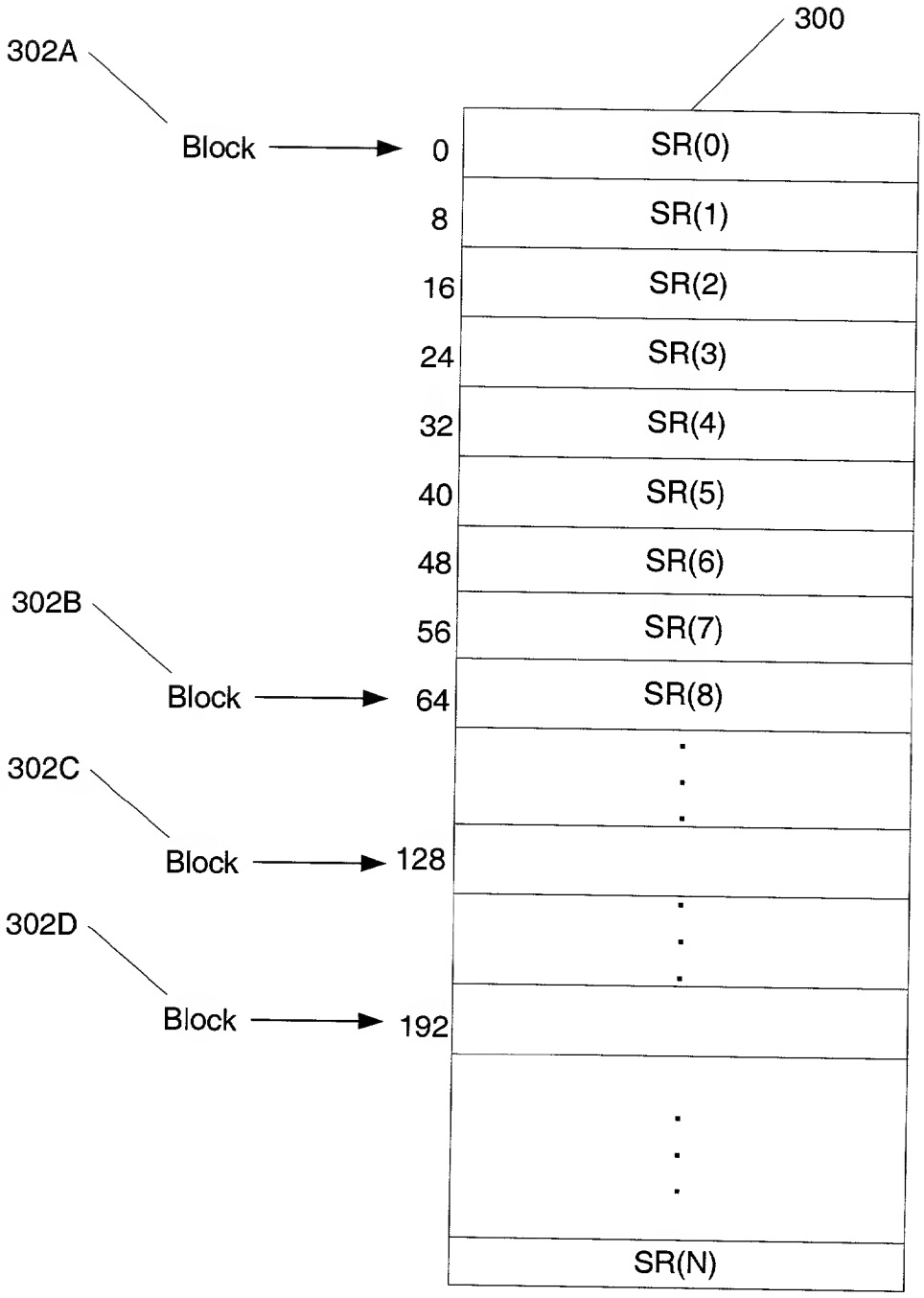
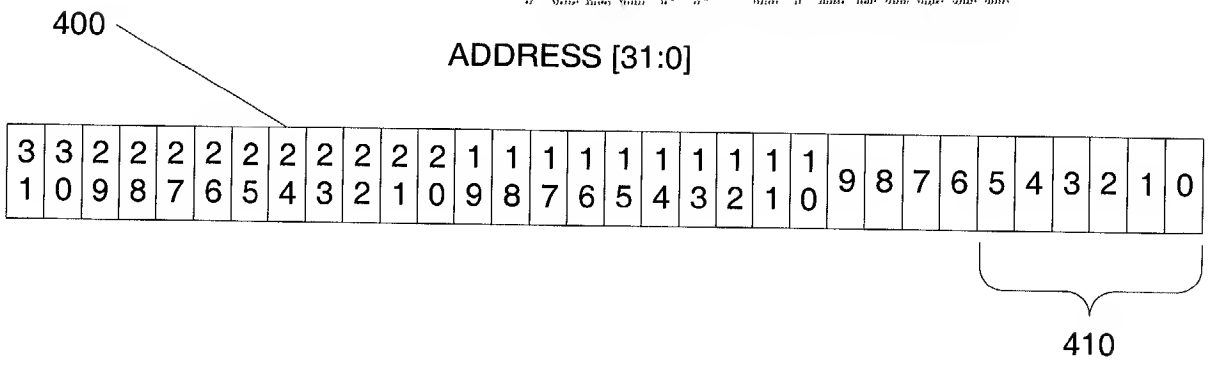

300
302A
Block
0
SR(0)
8
SR(1)
16
SR(2)
24
SR(3)
32
SR(4)
40
SR(5)
48
SR(6)
302B
56
SR(7)
Block
64
SR(8)
302C
Block
128
302D
Block
192
SR(N)

Fig. 3


400
ADDRESS [31:0]
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
410

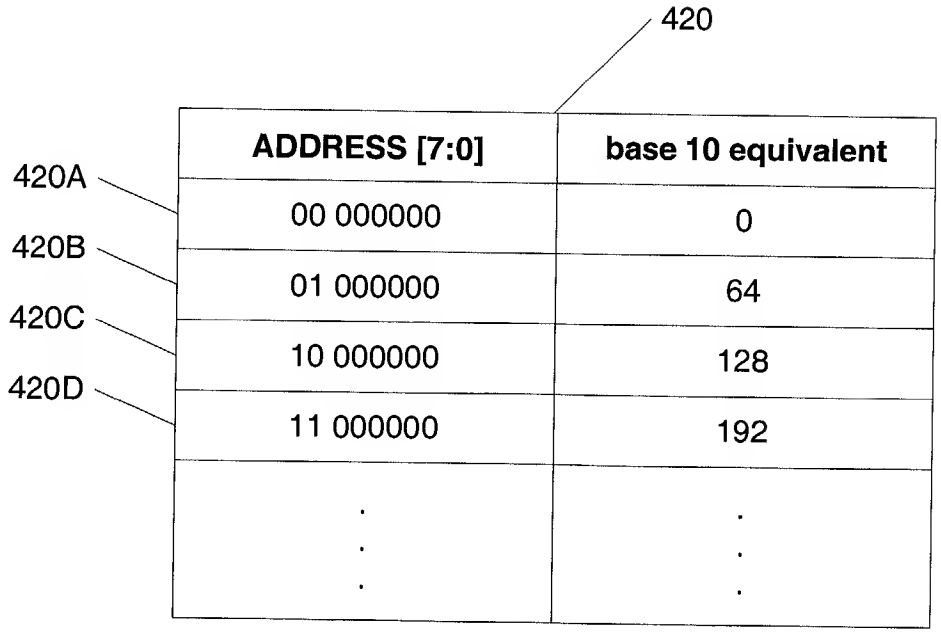
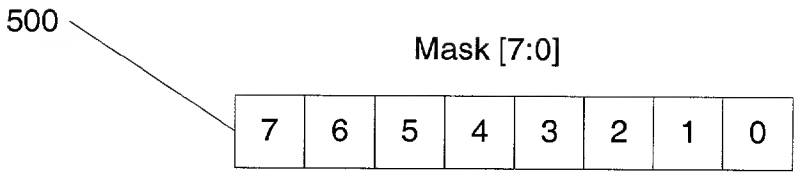

420
420A
420B
420C
420D
ADDRESS [7:0]
base 10 equivalent
00 000000
0
01 000000
64
10 000000
128
11 000000
192

Fig. 4



502

	Mask Bit	Block Bytes
504A	0	0-7
504B	1	8-15
504C	2	16-23
504D	3	24-31
504E	4	32-39
504F	5	40-47
504G	6	48-55
504H	7	56-63

Fig. 5

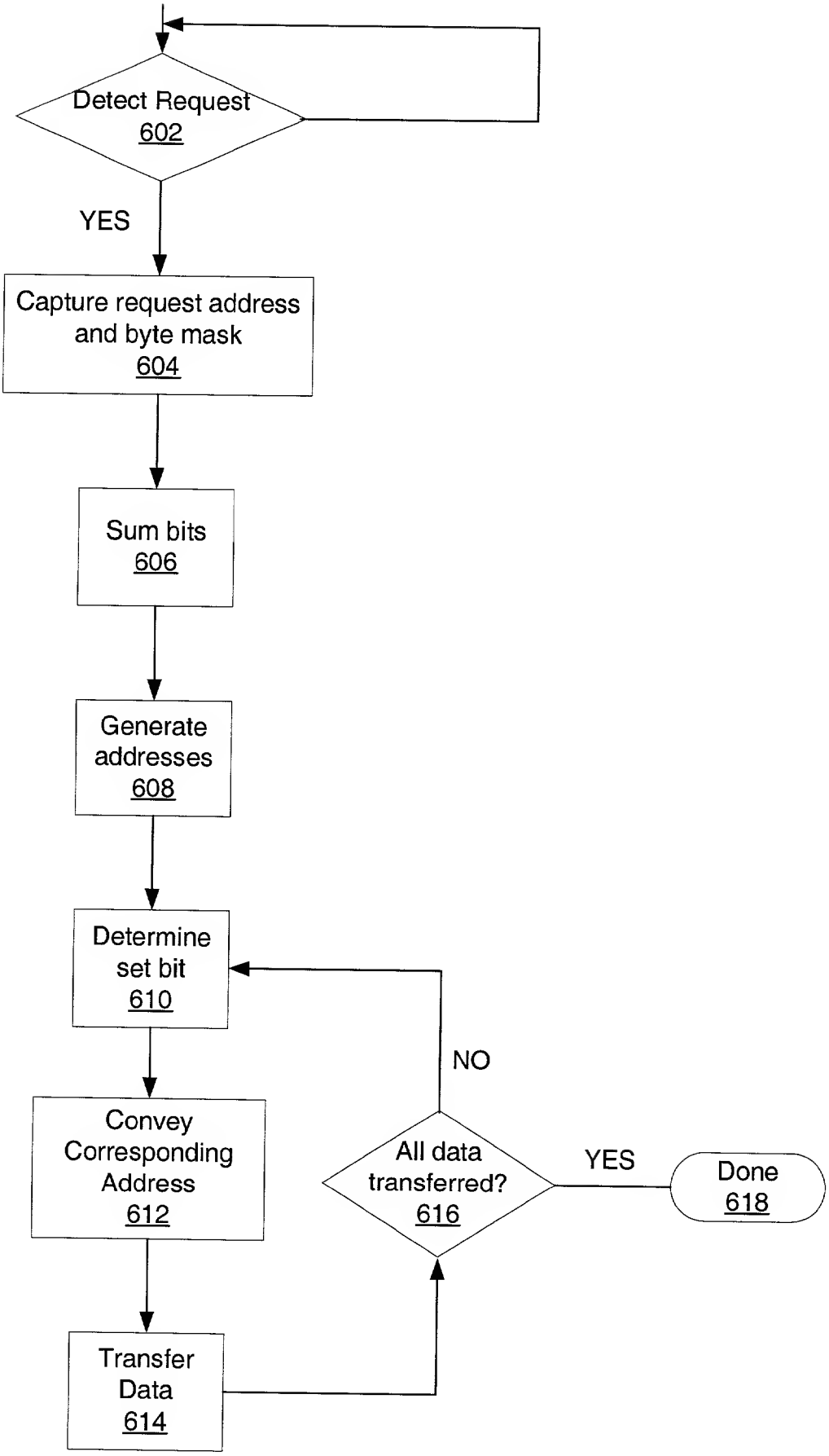

Detect Request
602
YES
Capture request address and byte mask
604
Sum bits
606
Generate addresses
608
Determine set bit
610
Convey Corresponding Address
612
Transfer Data
614
All data transferred?
616
NO
YES
Done
618

Fig. 6

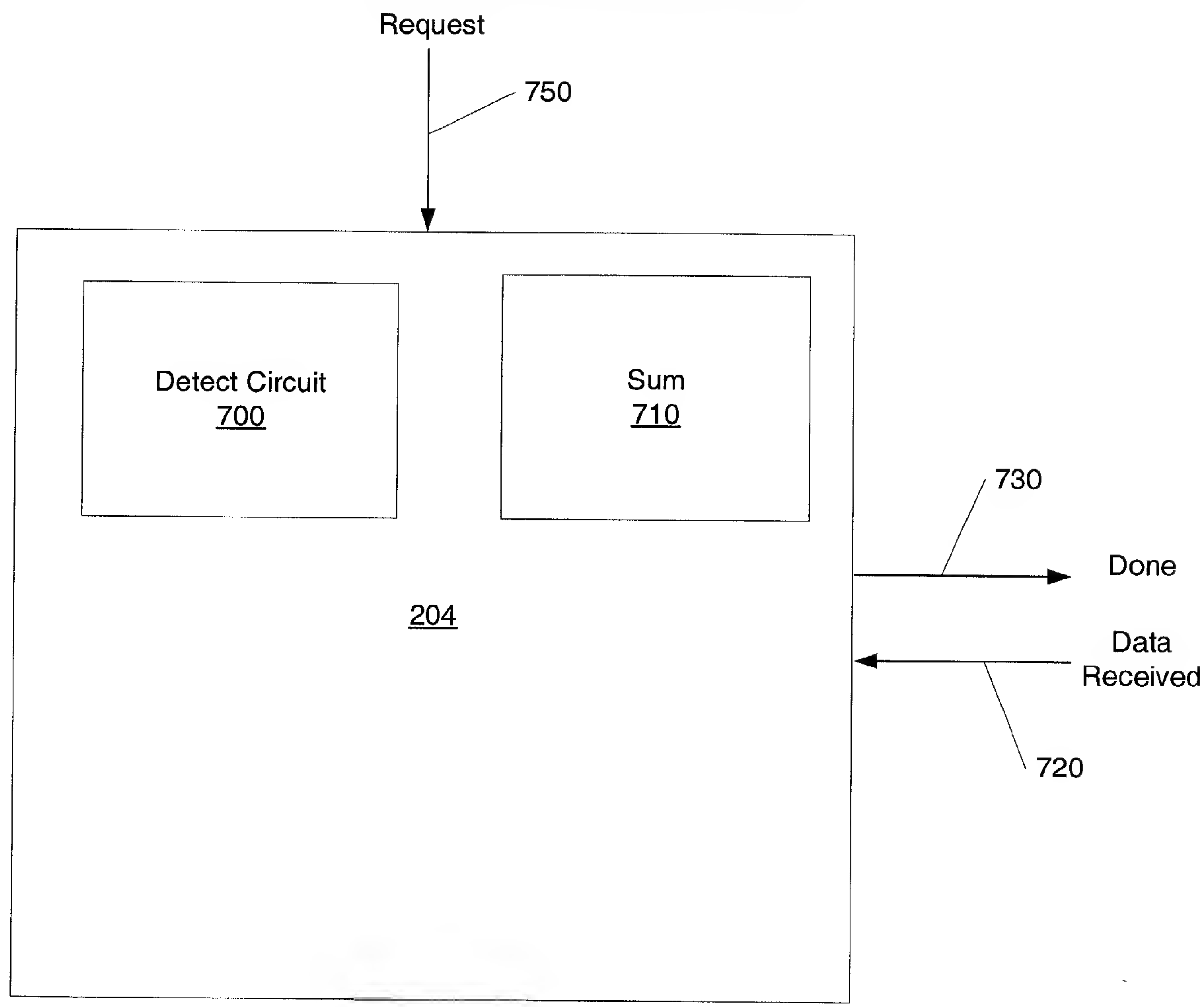

Request
750
Detect Circuit
700
Sum
710
204
730
Done
Data
Received
720

Fig. 7

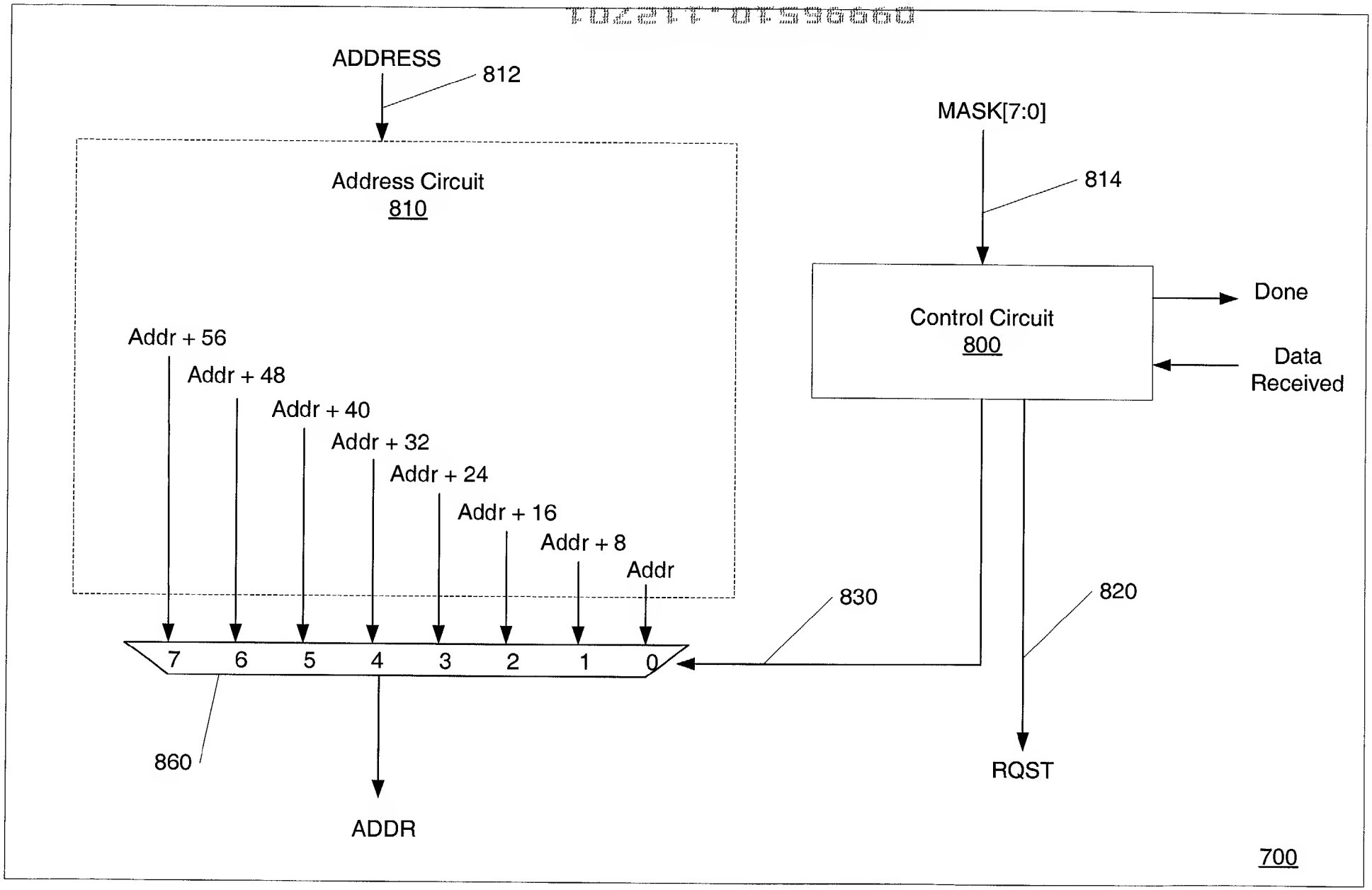

ADDRESS
812
MASK[7:0]
814
Address Circuit
810
Control Circuit
800
Done
Data
Received
Addr + 56
Addr + 48
Addr + 40
Addr + 32
Addr + 24
Addr + 16
Addr + 8
Addr
830
820
7
6
5
4
3
2
1
0
860
ADDR
RQST
700

Fig. 8

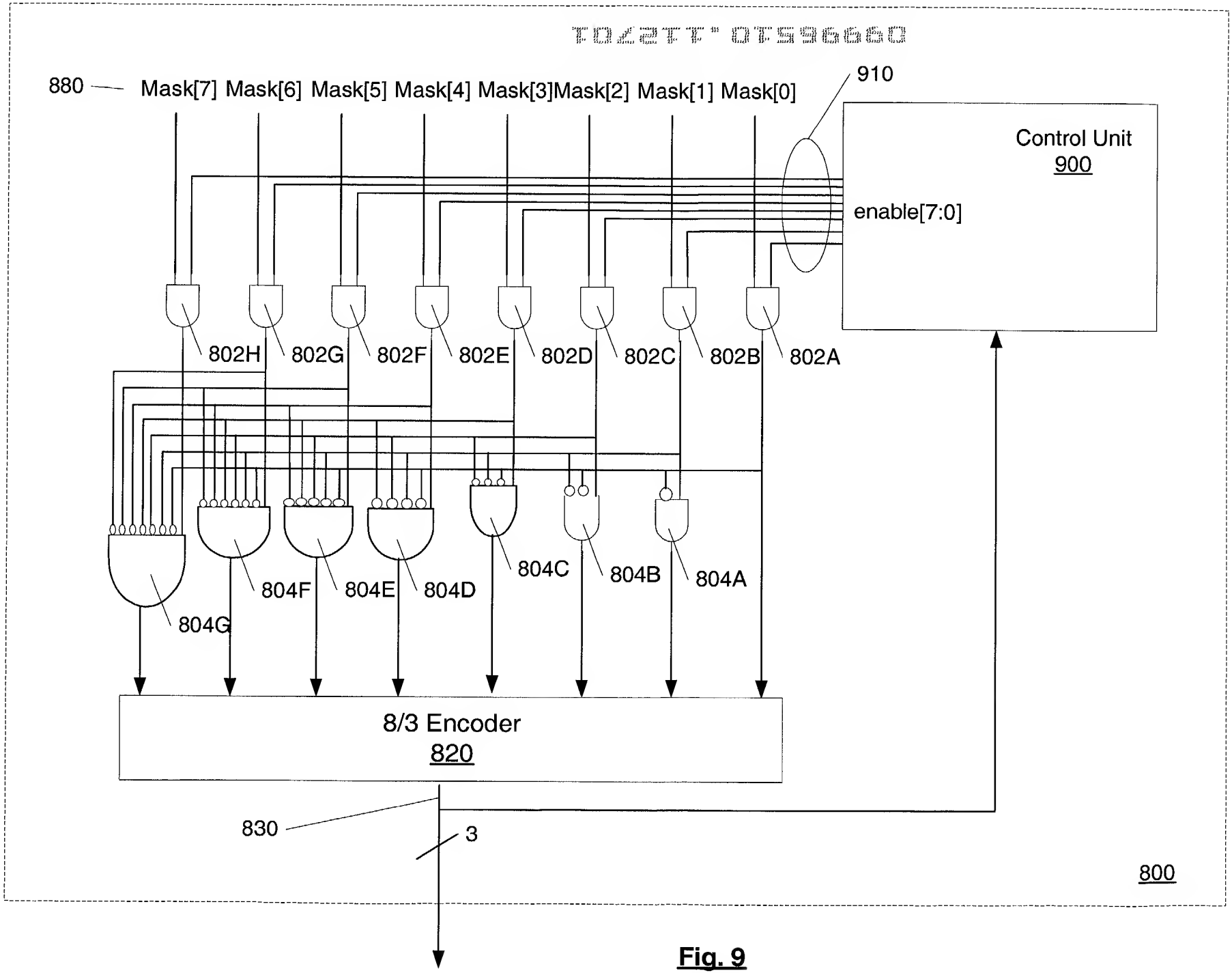
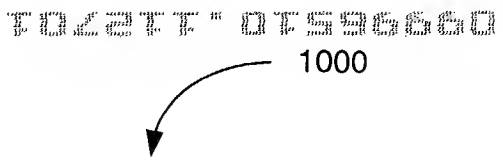

880
Mask[7] Mask[6] Mask[5] Mask[4] Mask[3]Mask[2] Mask[1] Mask[0]
910
Control Unit
900
enable[7:0]
802H
802G
802F
802E
802D
802C
802B
802A
804G
804F
804E
804D
804C
804B
804A
8/3 Encoder
820
830
3
800

Fig. 9



Iteration 1002	Enable[7:0] 1004	Mask[7:0] 1006	gates 802H-802A 1008	gates 804G-804A 1010	signal[2:0] 830 1012
0	11111111	01101000	01101000	00001000	011
1	11110000	01101000	01100000	00100000	101
2	11000000	01101000	01000000	01000000	110

Fig. 10